(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
1 September 2005 (01.09.2005)

PCT

(10) International Publication Number
WO 2005/079182 A3

(51) International Patent Classification[7]: H01L 29/786, 21/336, 21/8238

(21) International Application Number: PCT/US2004/001721

(22) International Filing Date: 22 January 2004 (22.01.2004)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

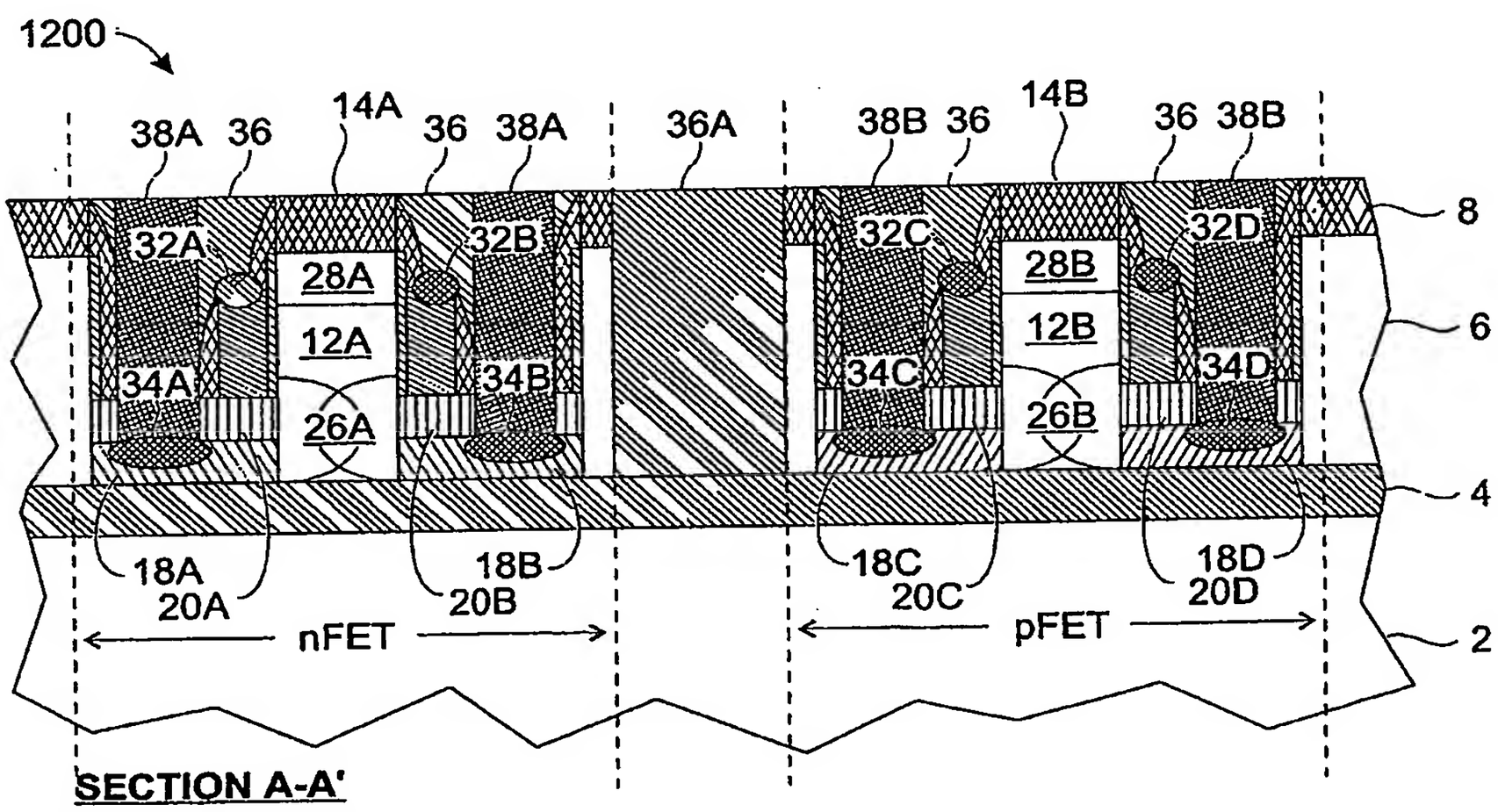
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:
— *of inventorship (Rule 4.17(iv))*

Published:
— *with international search report*

[Continued on next page]

(54) **Title:** VERTICAL FIN-FET MOS DEVICES



(57) **Abstract:** A new class of high-density, vertical Fin-FET devices that exhibit low contact resistance is described. These vertical Fin-FET devices have vertical silicon "fins" (12A) that act as the transistor body. Doped source and drain regions (26A, 28A) are formed at the bottoms and tops, respectively, of the fins (12A). Gates (24A, 24B) are formed along sidewalls of the fins. Current flows vertically through the fins (12A) between the source and drain regions (26A, 28A) when an appropriate bias is applied to the gates (24A, 24B). An integrated process for forming pFET, nFET, multi-fin, single-fin, multi-gate and double-gate vertical Fin-FETs simultaneously is described.

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(88) Date of publication of the international search report:
6 April 2006

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.